of the trench, to form the n drain drift region or p side wall region. In this case, the polycrystalline silicon filling the trench may be removed by etching, or may be oxidized to form an oxide film.

In the illustrated embodiments, it is also possible to change the conductivity type of the semiconductor regions of the MOSFET. Further, the gate insulating film is not limited to an oxide film, and therefore the present invention is also applicable to a MISFET having a MIS (metal-insulator-semiconductor) gate structure.

In the vertical trench MOSFET according to any of the first through third embodiments of the present invention, the first conductivity type drain drift region formed as a surface layer of the side wall of the trench has a relatively small thickness, and an impurity concentration that is higher than a level at which the breakdown voltage measured in a hypothetical diffusion type junction is substantially equal to the withstand voltage of the element. Upon application of voltage lower than the element withstand voltage, therefore, a depletion layer fills the first conductivity type drain drift region and the second conductivity type region, whereby positive and negative fixed charges in these regions are balanced or offset, to thus reduce the electric field and achieve a high withstand voltage. Further, the ON-state resistance of the vertical trench MISFET can be reduced because of the high impurity concentration of the first conductivity type drain drift region.

In the vertical trench MOSFET according to any of the fourth through sixth embodiments of the invention, the second conductivity type side wall region is formed as a surface layer of the side wall of the trench, and the first conductivity type impurity layer has an impurity concentration that is higher than a level at which the breakdown voltage measured in a hypothetical diffusion type junction is substantially equal to the withstand voltage of the element. Upon application of voltage lower than the element withstand voltage, therefore, a depletion layer fills the first conductivity type drain drift region and the second conductivity type side wall region, whereby positive and negative fixed charges in these regions are balanced, to thus reduce the electric field and achieve a high withstand voltage. Further, the ON-state resistance of the vertical trench MISFET can be reduced because of the high impurity concentration of the first conductivity type drain drift region.

With the impurity concentration of the drain drift region thus increased, the ON-state resistance of this region has a reduced temperature dependency, thus limiting an increase in the ON-state resistance of the element at a high temperature.

To achieve a desired the ON-state resistance, the size of the chip can be reduced according to the present invention, with a result of a reduced gate area and a reduce area of each junction, as compared with a conventional counterpart. Consequently, the parasitic capacity and the switching loss of the element can be advantageously reduced. Further, the manufacturing cost can be reduced with the reduction of the chip size.

What is claimed is:

1. A method of manufacturing a vertical trench MISFET, comprising the steps of:

preparing a semiconductor substrate having a first conductivity type semiconductor, and a second conductivity type impurity layer disposed on the first conductivity type semiconductor;

forming a trench extending from a surface of said semiconductor substrate to reach said first conductivity type semiconductor;

forming a second conductivity type base region in a top portion of said semiconductor substrate;

forming a first conductivity type source region in a part of a surface layer of said second conductivity type base region;

forming an impurity diffused layer by obliquely implanting ions into a side wall of said trench, which is then subjected to heat treatment, thereby to form a first conductivity type drain drift region in a surface layer of the side wall of the trench, said first conductivity type drain drift region having a first impurity concentration that is higher than a second impurity concentration at which a breakdown voltage measured in a hypothetical diffusion type junction is substantially equal to an element withstand voltage;

forming a gate electrode on an exposed surface of said second conductivity type base region, through a gate insulating film;

forming a source electrode in contact with surfaces of both of said first conductivity type source region and said second conductivity type base region; and

forming a drain electrode in contact with a rear surface of said first conductivity type semiconductor.

2. A method of manufacturing a vertical trench MISFET, comprising the steps of:

preparing a semiconductor substrate having a first conductivity type semiconductor, and a first conductivity type impurity layer provided on the first conductivity type semiconductor, said first conductivity type impurity layer having a first impurity concentration that is higher than a second impurity concentration at which a breakdown voltage measured in a hypothetical diffusion type junction is substantially equal to an element withstand voltage;

forming a trench extending from a surface of said semiconductor substrate to reach said first conductivity type semiconductor;

forming a second conductivity type base region in a top portion of said semiconductor substrate;

forming a first conductivity type source region in a part of a surface layer of said second conductivity type base region;

forming an impurity diffused layer by obliquely implanting ions into a side wall of said trench, which is then subjected to heat treatment, thereby to form a second conductivity type side wall region in a surface layer of the side wall of the trench;

forming a gate electrode on an exposed surface of said second conductivity type base region, through a gate insulating film;

forming a source electrode in contact with surfaces of both of said first conductivity type source region and said second conductivity type base region; and

forming a drain electrode in contact with a rear surface of said first conductivity type semiconductor.

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